**On-Chip Interconnection Network**

**CSEE 4340:**

**Computer Hardware Design**

**Fall 2012**

**SECTION 1:**

**Project Title: On-Chip Interconnection Network**

**Team Name:** Flit Busters

**Project Members:** Adil Sadik (ams2378)

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**Project Member Duties:**

**Design Team:**

* Adil Sadik (Master)
* Dechhin Lama

**Verification Team:**

* Ashwin Ramachandran (Master)
* Ayushi Rajeev

**Section 2:**

**Design Overview:**

In this project, we will be designing and testing a 4x4 on-chip interconnection network using SystemVerilog HDL.

As the number of IP-modules on System-On-Chip’s increases, bus based interconnections can no longer meet the necessary bandwidth, latency and power consumption requirements. As a solution for more efficient communication between the modules, Network-On-Chip’s are developed. NoC’s consist of routers that are connected to each IP-module. Routers are then connected in various topologies such that they can communicate to neighboring routers (nodes in a network) via handshaking protocol and pass messages addressed to a specific node.

For our project, we will be designing a 4x4 mesh network where packets (a unit of message comprising of one or more flits) are routed to various nodes of the network. Routers will examine the header flit and route the following flits to the desired destination. Since we are designing a 4x4 mesh network, each node will be assigned an X-Y co-ordinate in a two-dimensional grid. Messages addressed to a particular co-ordinate are then passed along the nodes of the network, first in the Y-axis followed by the X-axis. Each router (node) will have four input-output pairs connecting to neighboring routers and one input-output pair to the local module.

In order to prevent cases where a transmitting router sends data when the receiving end is not yet ready to accept, we will be using a Credit-based flow control. Here, each router will have a buffer queue for each input where packets are stored temporarily. The transmitting router will maintain a count on the number of free slots available on the receiving end and transmit data only when there are “credits” available.

We will begin our design such that only single header flits are routed. Once this is successfully implemented and tested, we will then extend our design such that the header flit is followed by 4 body flits that follow through with the header flit to the designated destination (i.e. Wormhole routing). Furthermore, we will optimize our design by modifying the routers on the edge of the network such that unnecessary ports are omitted.